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13. ABSTRACT (Maximum 200 words)

We have demonstrated the first GaN current aperture vertical electron transistor (CAVET). A 2 μm thick GaN:Si drain region followed by a 0.4 μm GaN:Fe insulating layer and an 800 \AA unintentionally doped GaN cap were grown by MOCVD on a c-plane sapphire substrate. Channel apertures were etched, and a maskless regrowth was performed to grow conducting GaN inside the channel as well as to thicken the UID GaN above the insulating layer and add an AlGaN cap layer. Cl₂ RIE was used to pattern the device mesa. Source, drain, and gate pads were then deposited. Devices with aperture widths ranging from 0.4 μm to 2 μm have been demonstrated. DC transistor characteristics were measured, and the effects of varying the aperture length and the gate overlap were investigated. Electrical characteristics of a device with a 0.6 μm aperture and a gate overlap of 2 μm are illustrated in Fig 2. This device had a source-drain saturation current of 430 mA/mm and an extrinsic transconductance of 100 mS/mm. Additionally, conditions for PEC etching of an InGaN layer for the CAVET illustrated in Fig 1d have been optimized.

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Final Report for Current Apertured Vertical Electron Transistor (CAVET)

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We have demonstrated the first GaN current aperture vertical electron transistor (CAVET). A 2 μm thick GaN:Si drain region followed by a 0.4 μm GaN:Fe insulating layer and an 800 Å unintentionally doped GaN cap were grown by MOCVD on a *c*-plane sapphire substrate. Channel apertures were etched, and a maskless regrowth was performed to grow conducting GaN inside the channel as well as to thicken the UID GaN above the insulating layer and add an AlGaN cap layer. Cl_2 RIE was used to pattern the device mesa. Source, drain, and gate pads were then deposited. Devices with aperture widths ranging from 0.4 μm to 2 μm have been demonstrated. DC transistor characteristics were measured, and the effects of varying the aperture length and the gate overlap were investigated. Electrical characteristics of a device with a 0.6 μm aperture and a gate overlap of 2 μm are illustrated in Fig 2. This device had a source-drain saturation current of 430 mA/mm and an extrinsic transconductance of 100 mS/mm. Additionally, conditions for PEC etching of an InGaN layer for the CAVET illustrated in Fig 1d have been optimized.

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I. INTRODUCTION

During the past few years, enormous progress has been made in the development of III-nitride semiconductor materials for optoelectronic devices in the green/blue/UV spectral ranges [1], [2] as well as for high voltage, high power, and high temperature electronics applications [3], [4]. Impressive demonstrations of AlGaIn/GaN high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) continue to be reported [3]-[5]. High breakdown field strength in GaN (2 MV/cm [6]) permits very high voltages to be sustained during operation of these devices. In HEMTs, breakdown results from an avalanche process that usually occurs near the gate edge on the drain side [7], where accumulation of charge at high gate-drain voltages results in large localized electric fields. Achieving a high breakdown voltage in a HEMT requires decreasing the electric field at the surface of the channel at the drain edge of the gate. In GaN HEMTs, this has been accomplished by Zhang *et al.* with the employment of an overlapping gate structure, and source-drain breakdown voltages of over 1 kV have been achieved [8].

Another approach to achieving large breakdown voltages is to employ a current aperture vertical electron transistor (CAVET) structure. As illustrated in Figs 1c and 1d, a CAVET consists of a source region separated from a drain region by an insulating layer containing a narrow aperture which is filled with conducting material. In the case of Fig 1c, the channel is UID GaN and the insulating layer is Fe-doped GaN, while in Fig 1d, the channel is InGaIn and the insulator is air. A device mesa is formed by reactive ion etching, and source contacts are deposited on either side of the aperture. The drain metal contacts the n-doped region below the aperture. Electrons flow from the source contacts through the aperture into the n-type GaN and are collected at the drain. A Schottky gate,

located directly above the aperture, is used to modulate the current passing through the aperture.

In a CAVET, because the virtual drain (or the pinched off region) is located underneath the gate, charge does not accumulate at the gate edge, so no large fields near the gate edge are present. Instead, our simulations show that the high field region in a CAVET is buried in the bulk. The CAVET therefore has the potential to support very large source-drain voltages, since surface related breakdown is eliminated. Additionally, when the device is optimized, surface related instabilities such as DC-RF dispersion should be mitigated.

For the device with the Fe-doped insulating region, a maskless regrowth is performed to grow the UID GaN channel as well as the UID GaN and AlGaN above the insulating layer. In the case of the InGaN channel CAVET, the entire epitaxial growth is performed, and then a photoelectric chemical (PEC) etch is used to selectively etch the InGaN until only a narrow InGaN channel remains. In this report, we discuss progress on both types of CAVETs.

II. REGROWN CHANNEL CAVETS

We have successfully fabricated and tested regrown channel AlGaN/GaN CAVETs. The device layer structure was grown by MOCVD on a *c*-plane sapphire substrate. The epitaxial growth began with a 2 μm n-type ($\sim 6 \times 10^{17} \text{ cm}^{-3}$ Si doped) GaN drain layer, followed by a 0.4 μm insulating ($\sim 1 \times 10^{18} \text{ cm}^{-3}$ Fe doped) GaN layer [9] and an 800 Å unintentionally doped (UID) GaN capping layer (see Fig. 1a). Next, channel

apertures were etched through the Fe-doped GaN by Cl_2 reactive ion etching (RIE), as illustrated in Fig 1b. The transistors had aperture lengths L_{ap} of 0.4 μm , 0.6 μm , 1 μm , 1.5 μm , and 2 μm . The wafer was then placed back into the MOCVD chamber and a maskless regrowth was performed. 1700 Å of UID GaN was grown, followed by a 225 Å $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$ cap, resulting in the structure shown in Fig. 1c. Interrupted growth studies indicate that the aperture partially fills with GaN while the sample is heated during the regrowth process as a result of mass transport of material from the surface into the aperture. The surface directly above the apertures did not entirely planarize during the regrowth; a small depression could still be observed, as illustrated in Fig. 1c. A two-dimensional electron gas (2DEG) is present in the GaN near the AlGaIn/GaN heterointerface, enabling the formation of ohmic source contacts and providing the charge that is collected at the drain.

After the regrowth was performed, a device mesa for the source and gate region was formed with Cl_2 RIE. $\text{Ti}/\text{Al}/\text{Ni}/\text{Au}$ (200/2200/550/450 Å) were then evaporated and annealed at 870 °C for 30 s to form ohmic source and drain contacts. The source metal contacts the 2DEG near the AlGaIn/GaN heterointerface, while the drain metal contacts the Si-doped GaN layer at the base of the structure. The final step of the process was to evaporate Ni/Au (300/3500 Å) for a gate metallization. Devices with various aperture lengths (L_{ap}) and gate overlapping lengths (L_{go}) were fabricated to investigate their effects on device performance. All devices had a gate-source spacing (L_{gs}) of 1.5 μm , a gate width (W_g) of 100 μm , and a total source width of 200 μm (100 μm per source pad).

A Tektronix 370A programmable curve tracer was used to perform the electrical characterization of these devices. The dc I_{ds} - V_{ds} characteristics of a device with $L_{ap} = 0.6$

μm and $L_{go} = 2 \mu\text{m}$ are illustrated in Fig. 2. The maximum value of drain current (I_{dss}) of this device is 430 mA/mm and the extrinsic transconductance (g_m) is $\sim 100 \text{ mS/mm}$ at $I_{ds} \sim 350 \text{ mA/mm}$ and $V_{ds} \sim 10 \text{ V}$. The pinch-off voltage V_p of this device is -4 V . A parasitic leakage current $I_{leakage}$ which increases with larger V_{ds} is present in every device. We believe the leakage current results from electrons moving through both the UID GaN underneath the 2DEG as well as through the iron-doped layer, as indicated in Fig. 1c. Unlike the current which originates from the 2DEG, the leakage current is not modulated by the gate.

Devices with a gate overlap length L_{go} of $2 \mu\text{m}$ and aperture lengths L_{ap} ranging from $0.4 \mu\text{m}$ to $2 \mu\text{m}$ were all found to have identical electrical characteristics to those of the device in Fig. 2, indicating that the maximum current I_{dss} in these devices is limited by the available charge in the 2DEG and not by the aperture. However, both I_{dss} and $I_{leakage}$ do depend on the gate overlap L_{go} . Fig. 3 shows a plot of I_{dss} and $I_{leakage}$ for devices with aperture length $L_{ap} = 1 \mu\text{m}$ and L_{go} varying from $0.6 \mu\text{m}$ to $2 \mu\text{m}$. $I_{leakage}$ was taken to be the total source-drain current while the device was pinched off ($V_g = -4 \text{ V}$) and $V_{ds} = 10 \text{ V}$. As L_{go} is decreased, I_{dss} increases, but the leakage current at pinch-off increases as well. The gate overlap length L_{go} in the CAVET is analogous to the effective gate length in a standard FET. The observed increase in leakage current for smaller values of L_{go} results from short channel effects, similar to those in a standard FET.

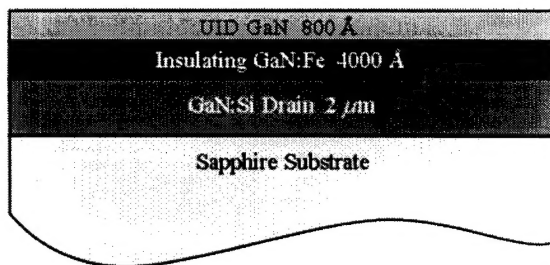
III. INGAN CHANNEL CAVETS (UTILIZING PEC ETCH)

An alternative way to fabricate CAVETs is to form the aperture by Photoelectrochemical selective etching. The imagined structure of device is shown in Fig1d. Photoelectrochemical wet etching [10,11] has been an efficient way to selectively etching InGaN (lower bandgap material) over GaN(higher bandgap material). The principal issues here regard achieving a sufficiently smooth etched surface. In order to achieve this, we have carried out a series of Taguchi experiments, varying intensity, bias and KOH concentration. Photoelectrochemical etching set-up is shown in Fig4. Xe lamp is used as the lamp source. Etching solution is aqueous potassium hydroxide. Bias is applied between anode (our sample) and cathode (Pt wire). In order to get the selective etching InGaN layer between GaN, one as-grown MOCVD GaN template on sapphire is used as filter to insert between lamp source and sample. Thus, only the photons with smaller energy than GaN will be permitted to reach sample, generate electron-hole pairs in the InGaN layer, this gives selective etching. Taguchi method is used to efficiently optimize the etching parameters to achieve the smoothest undercut with the highest etching selectivity. Based on our Taguchi result, the low concentration of KOH is found to be a critical factor for the smooth undercut surface. Fig5 give the etching morphology under optimized etching condition (600W lamp power, 0.55M KOH, 2.75V applied bias, 3min etching time). Further decrease the concentration of KOH, the undercut of InGaN over GaN can be controlled well. Fig6 shows the aperture formed by etching $\text{In}_x\text{Ga}_{1-x}\text{N}$ (600\AA , $x\sim 8\%$) under 0.01M KOH solutions. So with the etch we understood and optimized now, we will proceed to fabricate and characterize the CAVET structures.

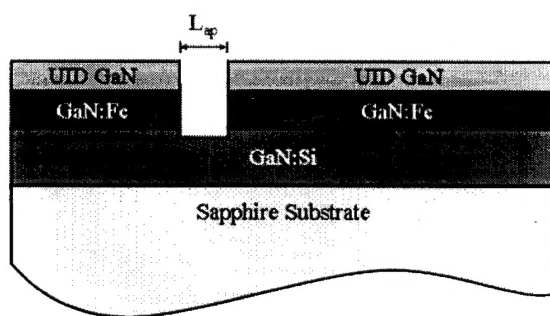
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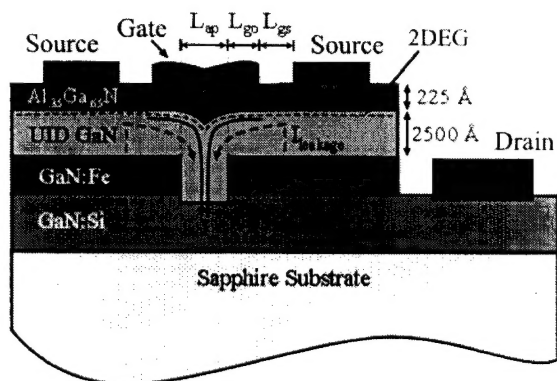
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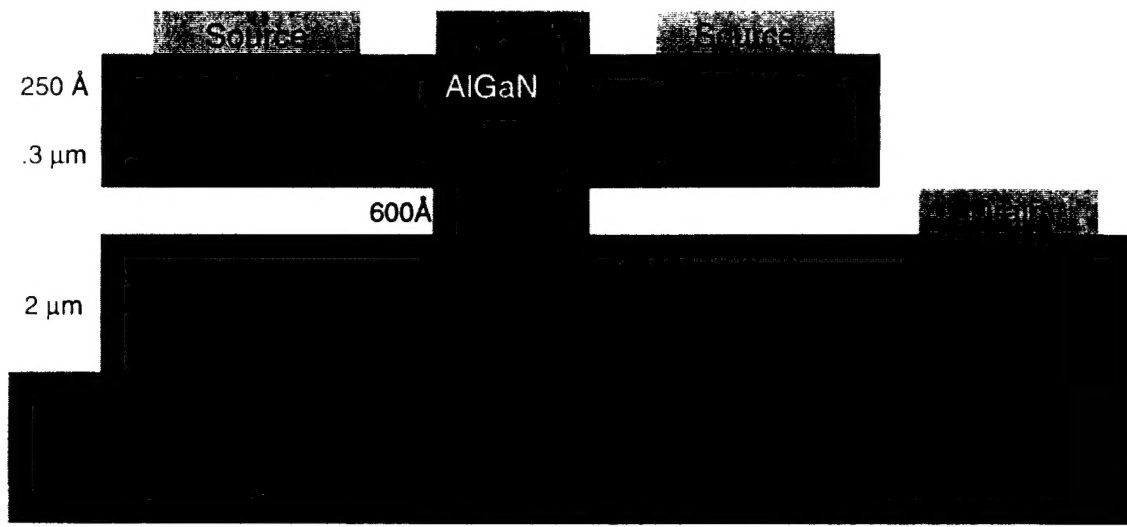
l(a)



l(b)



l(c)



1(d)

Fig. 1. Schematic diagrams of (a) initial layer structure, (b) aperture etch, and (c) completed regrown channel CAVET. A schematic diagram of an InGaN channel CAVET is shown in (d).

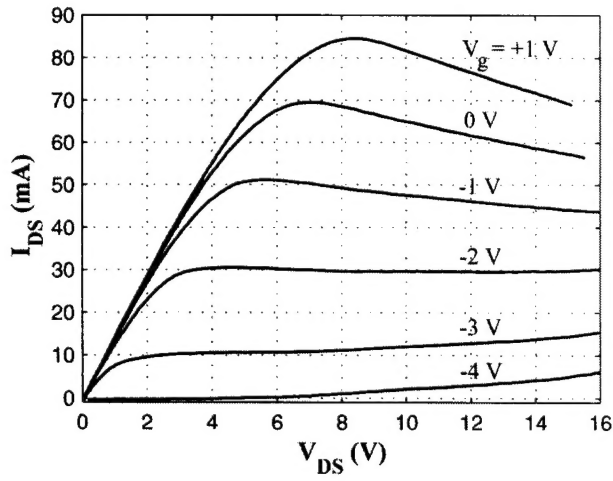


Fig. 2. I_{ds} - V_{ds} characteristics of a CAVET with gate width $W_g = 100 \mu\text{m}$, aperture length $L_{ap} = 0.6 \mu\text{m}$, and gate overlap $L_{go} = 2 \mu\text{m}$.

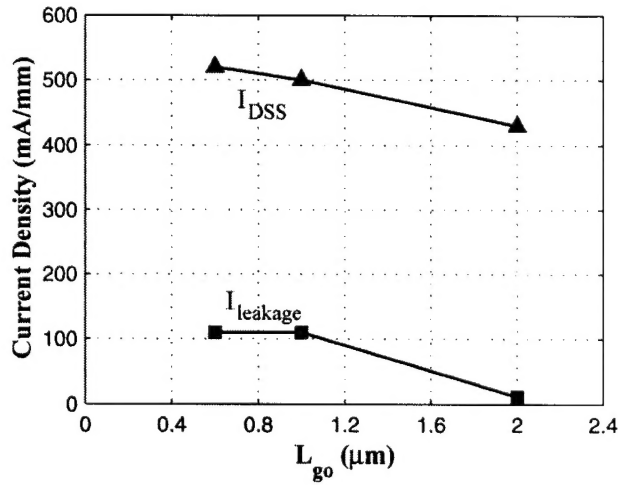


Fig. 3. Dependency of saturation current and leakage current on different values of gate overlap L_{go} . Here leakage current is defined to be the total source-drain current while the device was pinched off ($V_g = -4 \text{ V}$) and $V_{ds} = 10 \text{ V}$.

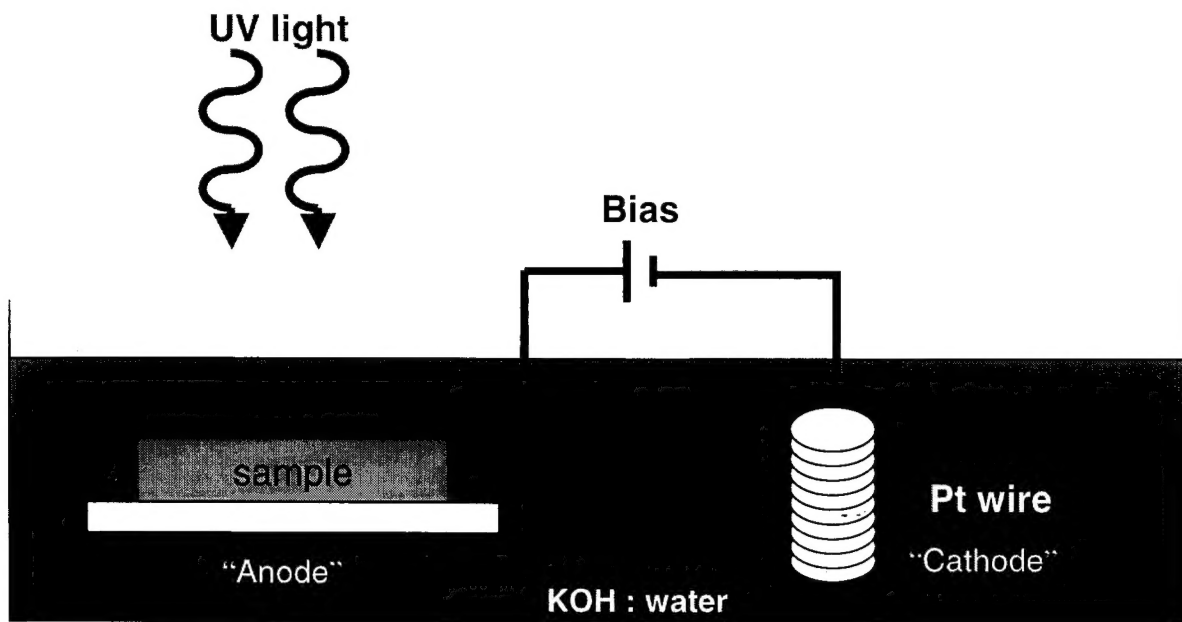


Fig 4. Photoelectrochemical wet etching set-up. The etching parameters are lamp power, applied bias, and concentration of KOH solution.

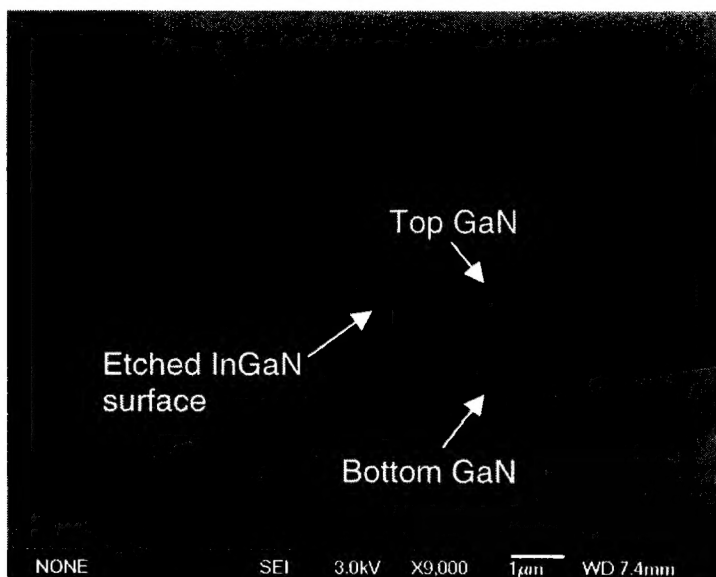


Figure 5. The smooth undercut under the optimized etching condition by Taguchi method.

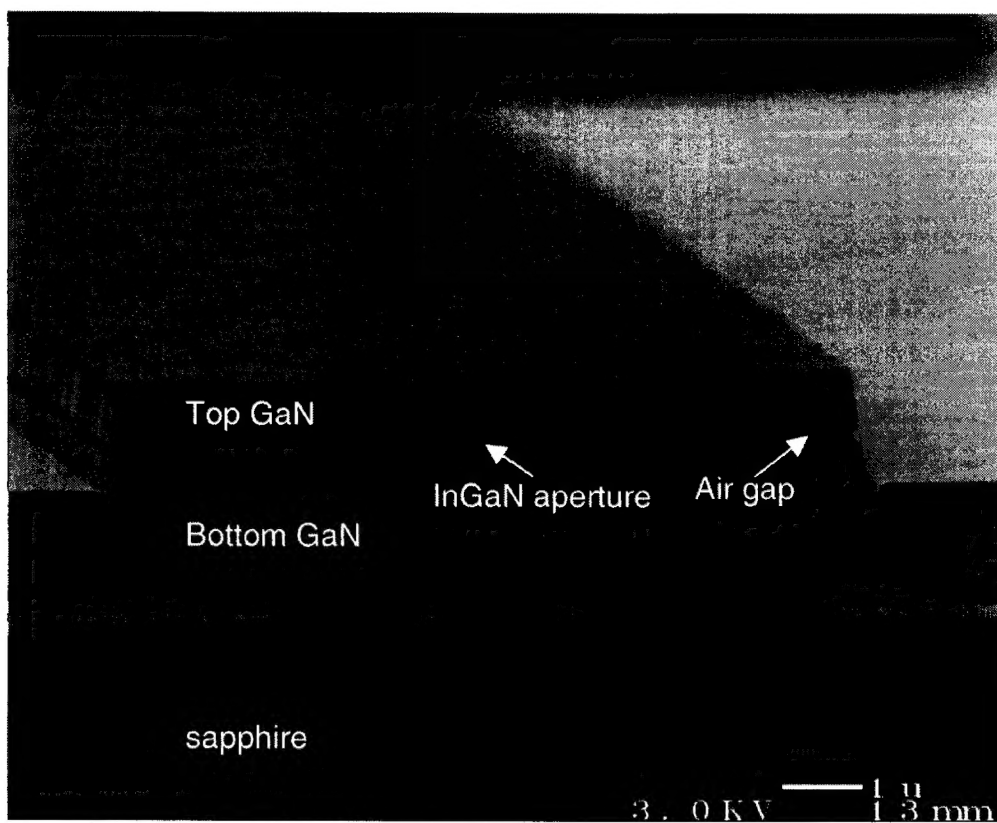


Fig 6. Highly controllable aperture formed by lateral etching $\text{In}_x\text{Ga}_{1-x}\text{N}$ ($x \sim 8\%$, 600 Å thick) sacrificial layer from each side.